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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,871	03/10/2004	Wei-Pang Huang	250122-1390	2230

24504 7590 04/16/2007

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EXAMINER	
DHARIA, PRABODH M	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,871	HUANG, WEI-PANG	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

2. **Status:** Please all the replies and correspondence should be addressed to examiner's new art unit 2629. Receipt is acknowledged of papers submitted on 03-10-2004 under a new application, which have been placed of record in the file. Claims 1-20 are pending in this action.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 9-12,15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Gleason Robert E. (US 6,392,617 B1).

Regarding Claim 1, Gleason Robert E teaches a detectable flat panel display (Col. 1, Line 12, Col. 3, Lines 35-39), comprising: a substrate including a circuit region (Col. 7, Lines 59-67, Col. 1, Lines 33-43, Col. 1, Line 18) and a display region (Col. 7, Lines 52-67, , Col. 1, Lines 33-43, Col. 1, Line 18); a circuit device disposed on the circuit region of the substrate; a display device disposed in the display region of the substrate (Col. 7, Lines 52-67, Col. 1, Line 18); and a metal pattern formed in the circuit region (Col. 7, Lines 59-67), capable of reflecting light such that the reflected light is detectable by recognition equipment (Col. 7, Lines 53-67).

Regarding Claim 2, Gleason Robert E teaches the circuit device is a thin film transistor (Col. 8, Lines 45-51).

Regarding Claim 3, Gleason Robert E teaches the display device is an organic light-emitting diode (Col. 8, Lines 38,39,45,46).

Regarding Claim 9, Gleason Robert E teaches layer above the metal pattern is transparent (Col. 7, Lines 59-64).

Regarding Claim 10, Gleason Robert E teaches the metal pattern is the outermost layer (Col. 7, Lines 59-64).

Regarding Claim 11, Gleason Robert E teaches a detectable flat panel display (Col. 1, Line 12, Col. 3, Lines 35-39), comprising: a substrate including a circuit region (Col. 7, Lines 59-67, Col. 1, Lines 33-43, Col. 1, Line 18) and a display region (Col. 7, Lines 52-67, , Col. 1, Lines 33-43, Col. 1, Line 18); a circuit device disposed on the circuit region of the substrate; a display device disposed in the display region of the substrate (Col. 7, Lines 52-67, Col. 1, Line 18); and a metal pattern formed in the circuit region (Col. 7, Lines 59-67), capable of reflecting light such that the reflected light is detectable by recognition equipment (Col. 7, Lines 53-67).

Regarding Claim 12, Gleason Robert E. teaches the display device is an organic light-emitting diode (Col. 8, Lines 38,39,45,46).

Regarding Claim 15, Gleason Robert E teaches layer above the metal pattern is transparent (Col. 7, Lines 59-64).

Regarding Claim 16, Gleason Robert E teaches the metal pattern is the outermost layer (Col. 7, Lines 53-64).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-8,13,14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gleason Robert E. (US 6,392,617 B1) as applied to claim1-3, 9-12,15 and 16 above, and further in view of Yamazaki et al. (US 20030075733 A1).

Regarding Claim 4, Gleason Robert E teaches a substrate including a thin film transistor (TFT) region (Col. 7, Lines 59-67, Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 45-51) and an organic light-emitting diode (OLED) region (Col. 7, Lines 52-67, , Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 38,39,45,46); a thin film transistor disposed in the TFT region of the substrate (Col. 7, Lines 59-67, Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 45-51).

However, Gleason Robert E fails to recite or disclose the thin film transistor has a metal electrode as the metal pattern; a planarizing insulating layer covering the thin film transistor,

wherein the planarizing insulating layer has a contact window to expose the metal pattern; a transparent anode disposed in the OLED region of the substrate and electrically connected to the metal pattern; a transparent insulating cover layer covering a portion of the anode in a contact window position; an organic light-emitting layer disposed on the anode and the insulating cover layer; and a transparent cathode disposed on the organic light-emitting layer.

However, Yamazaki et al.discloses a substrate including a thin film transistor (TFT) region (page 1, paragraph 5, Lines 8-11, page 6, paragraph 128, Lines 3-6) and an organic light-emitting diode (OLED) region (page 1, paragraph 5, Lines 8-11, paragraph 6, page 6, paragraph 128, Lines 3-6); a thin film transistor disposed in the TFT region of the substrate (page 1, paragraph 5, Lines 8-11, paragraph 6, page 6, paragraph 128, Lines 3-6); the thin film transistor has a metal electrode as the metal pattern (page 5, paragraph 115, Lines 1-3, paragraph 116, Line 1,2); a planarizing insulating layer covering the thin film transistor (page 8, paragraphs 141,145,147) wherein the planarizing insulating layer has a contact window to expose the metal pattern (page 8, paragraphs 141,145,147, page 9, paragraph 164); a transparent anode disposed in the OLED region of the substrate (page 4, paragraph 76, page 15, paragraph 269) and electrically connected to the metal pattern (page 2, paragraph 18, page 11, paragraphs 21,212, page 5, paragraph 115, Lines 1-3, paragraph 116, Line 1,2); a transparent insulating cover layer covering a portion of the anode in a contact window position (page 15, paragraphs 268,269); an organic light-emitting layer disposed on the anode and the insulating cover layer (page 4, paragraph 76, page 15, paragraph 269); and a transparent cathode disposed on the organic light-emitting layer (page 4, paragraph 76, page 15, paragraph 268,269).

The reason to combine Yamazaki teaches specifically regions functioning as channels (channel formation regions) of plural thin film transistors in a pixel are arranged so as to have the same channel length direction and the channel length direction is matched to the scanning direction in laser light irradiation; therefore the crystal growth direction coincides with the carrier moving direction and high field effect mobility can be obtained.; TFT characteristics can be improved (specifically, increase in ON current and reduction in OFF current) and fluctuation in characteristic among TFTs can be reduced. In particular, fluctuation in ON current (I.sub.on) of a TFT that is electrically connected to an EL element in a pixel to supply a current to the EL element can be reduced (page 25, paragraph 440,441).

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Yamazaki et al. in the teaching of Gleason Robert E to be able to have OLED display fluctuation of the luminance between light emitting element can be reduced with respect to change in the environment; specifically change in the temperature.

Regarding Claim 5, Yamazaki et al. teaches the metal pattern is a source electrode or a drain electrode (page 5, paragraph 115, page 9, paragraphs 164,170, page 13, paragraph 246 teaches drain and gate electrodes are made of same material as gate electrode; metal).

Regarding Claim 6, Yamazaki et al. teaches the metal pattern is a gate (page 5, paragraph 115, page 9, paragraphs 164,170, page 13, paragraph 246 teaches drain and gate electrodes are made of same material as gate electrode; metal).

Regarding Claim 7, Yamazaki et al. teaches the planarizing insulating layer is a photoresist material or a dielectric material (page 8, paragraphs 141,145,147, 156).

Regarding Claim 8, Yamazaki et al. teaches the planarizing insulating layer is formed by spin coating (page 8, paragraphs 141,145,147, 156, page 14, paragraph 258).

Regarding Claim 13, Yamzaki et al. the organic light-emitting diode includes: an anode; an organic light-emitting layer disposed on the anode; a transparent cathode disposed on the light-emitting layer, wherein at least one of the organic light-emitting layer and the transparent cathode has an opening, and the metal pattern is disposed in the opening. (page 4, paragraph 76, page 15, paragraph 268,269).

Regarding Claim 14, Yamazaki et al. teaches a substrate including a thin film transistor (TFT) region (page 1, paragraph 5, Lines 8-11, page 6, paragraph 128, Lines 3-6) and an organic light-emitting diode (OLED) region (page 1, paragraph 5, Lines 8-11, paragraph 6, page 6, paragraph 128, Lines 3-6); a thin film transistor disposed in the TFT region of the substrate (page 1, paragraph 5, Lines 8-11, paragraph 6, page 6, paragraph 128, Lines 3-6); the thin film transistor has a metal electrode as the metal pattern (page 5, paragraph 115, Lines 1-3, paragraph 116, Line 1,2); a planarizing insulating layer covering the thin film transistor (page 8, paragraphs 141,145,147) wherein the planarizing insulating layer has a contact window to expose the metal pattern (page 8, paragraphs 141,145,147, page 9, paragraph 164); the source electrode, and the

drain electrode; an anode disposed in the OLED region of the substrate (page 4, paragraph 76, page 15, paragraph 269) and electrically connected to the gate the source electrode, and the drain electrode (page 8, paragraphs 141,145,147, 156, page 14, paragraph 258); and electrically connected to the metal pattern (page 2, paragraph 18, page 11, paragraphs 21,212, page 5, paragraph 115, Lines 1-3, paragraph 116, Line 1,2); a transparent insulating cover layer covering a portion of the anode in a contact window position (page 15, paragraphs 268,269); an organic light-emitting layer disposed on the anode and the insulating cover layer (page 4, paragraph 76, page 15, paragraph 269); and a transparent cathode disposed on the organic light-emitting layer (page 4, paragraph 76, page 15, paragraph 268,269).

Regarding Claim 17, Gleason Robert E. teaches detectable organic light-emitting diode display (Col. 7, Lines 53-64, Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 38,39,45,46), including a thin film transistor (TFT) region (Col. 7, Lines 59-67, Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 45-51) and an organic light-emitting diode (OLED) region (Col. 7, Lines 52-67, Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 38,39,45,46); a thin film transistor disposed in the TFT region of the substrate (Col. 7, Lines 59-67, Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 45-51).

However, Gleason Robert E fails to recite or disclose the thin film transistor has a metal electrode as the metal pattern; a planarizing insulating layer covering the thin film transistor, wherein the planarizing insulating layer has a contact window to expose the metal pattern; a transparent anode disposed in the OLED region of the substrate and electrically connected to the metal pattern; a transparent insulating cover layer covering a portion of the anode in a contact

window position; an organic light-emitting layer disposed on the anode and the insulating cover layer; and a transparent cathode disposed on the organic light-emitting layer.

However, Yamazaki et al. discloses a substrate including a thin film transistor (TFT) region (page 1, paragraph 5, Lines 8-11, page 6, paragraph 128, Lines 3-6) and an organic light-emitting diode (OLED) region (page 1, paragraph 5, Lines 8-11, paragraph 6, page 6, paragraph 128, Lines 3-6); a thin film transistor disposed in the TFT region of the substrate (page 1, paragraph 5, Lines 8-11, paragraph 6, page 6, paragraph 128, Lines 3-6); the thin film transistor has a metal electrode as the metal pattern (page 5, paragraph 115, Lines 1-3, paragraph 116, Line 1,2); a planarizing insulating layer covering the thin film transistor (page 8, paragraphs 141,145,147) wherein the planarizing insulating layer has a contact window to expose the metal pattern (page 8, paragraphs 141,145,147, page 9, paragraph 164); a transparent anode disposed in the OLED region of the substrate (page 4, paragraph 76, page 15, paragraph 269) and electrically connected to the metal pattern (page 2, paragraph 18, page 11, paragraphs 21,212, page 5, paragraph 115, Lines 1-3, paragraph 116, Line 1,2); a transparent insulating cover layer covering a portion of the anode in a contact window position (page 15, paragraphs 268,269); an organic light-emitting layer disposed on the anode and the insulating cover layer (page 4, paragraph 76, page 15, paragraph 269); and a transparent cathode disposed on the organic light-emitting layer (page 4, paragraph 76, page 15, paragraph 268,269).

The reason to combine Yamazaki teaches specifically regions functioning as channels (channel formation regions) of plural thin film transistors in a pixel are arranged so as to have the same channel length direction and the channel length direction is matched to the scanning direction in laser light irradiation; therefore the crystal growth direction coincides with the

carrier moving direction and high field effect mobility can be obtained.; TFT characteristics can be improved (specifically, increase in ON current and reduction in OFF current) and fluctuation in characteristic among TFTs can be reduced. In particular, fluctuation in ON current (I.sub.on) of a TFT that is electrically connected to an EL element in a pixel to supply a current to the EL element can be reduced (page 25, paragraph 440,441).

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Yamazaki et al. in the teaching of Gleason Robert E to be able to have OLED display fluctuation of the luminance between light emitting element can be reduced with respect to change in the environment; specifically change in the temperature.

6. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gleason Robert E. (US 6,392,617 B1). as applied to claims 1-3, 9-12,15 and 16 above, and further in view of Andry et al. (US 20030094894 A1)

Regarding Claim 18, Gleason Robert E. teaches detectable organic light-emitting diode display (Col. 7, Lines 53-64, Col. 1, Lines 33-43, Col. 1, Line 18; Col. 8, Lines 38,39,45,46), including a thin film transistor (TFT) region (Col. 7, Lines 59-67, Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 45-51) and an organic light-emitting diode (OLED) region (Col. 7, Lines 52-67, Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 38,39,45,46); a thin film transistor disposed in the TFT region of the substrate (Col. 7, Lines 59-67, Col. 1, Lines 33-43, Col. 1,

Line 18, Col. 8, Lines 45-51) and capable of reflecting light such that the reflected light is detectable by recognition equipment (Col. 7, Lines 53-64).

However, Gleason Robert E fails to recite or disclose an anode disposed in the OLED region of the substrate; an organic light-emitting diode disposed on the anode; and a transparent cathode disposed on the organic light-emitting layer, wherein at least one of the organic light-emitting layer and the transparent cathode has an opening, and a second metal pattern is disposed in the opening, capable of reflecting light.

However, Andry et al. discloses an anode disposed in the OLED region of the substrate; an organic light-emitting diode disposed on the anode; and a transparent cathode disposed on the organic light-emitting layer (page 2, paragraph 17, paragraph 18, Lines 1-3), wherein at least one of the organic light-emitting layer and the transparent cathode has an opening, and a second metal pattern is disposed in the opening, capable of reflecting light (page 2, paragraph 21, Lines 12-15, page 3, paragraph 22 Lines 1-13 teaches cathode also can reflect light).

The reason to combine Andry et al. teaches (AMOLED) dispalyswhich are enhanced by passivating the entire active array surface with an insulating layer, thereby substantially reducing or eliminating electrical shorts across the organic light emitting diode (OLED) layer from the top electrode to the bottom electrode.

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Andry et al. in the teaching of Gleason Robert E. to be able to have OLED display reducing or eliminating electrical shorts across the organic light emitting diode (OLED) layer from the top electrode to the bottom electrode (page 1, paragraph 2).

Regarding Claim 19, Gleason Robert E teaches a recognition system (Col. 8, Lines 3-15) detectable organic light-emitting diode display (Col. 7, Lines 53-64, , Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 38,39,45,46), including a thin film transistor (TFT) region (Col. 7, Lines 59-67, Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 45-51) and an organic light-emitting diode (OLED) region (Col. 7, Lines 52-67, Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 38,39,45,46); a thin film transistor disposed in the TFT region of the substrate (Col. 7, Lines 59-67, Col. 1, Lines 33-43, Col. 1, Line 18, Col. 8, Lines 45-51) and capable of reflecting light such that the reflected light is detectable by recognition equipment. (Col. 7, Lines 53-64); wherein the detectable flat panel display meets at least one of the following requirements: a first metal pattern is disposed in the circuit region, wherein any layer above the first metal pattern is transparent or the first metal pattern is the outermost layer, such that the first metal pattern is detectable by the recognition equipment (Col. 7, Lines 51-to Col. 8, Lines 18).

However, Gleason Robert E fails to disclose a second metal pattern is disposed in the display region, wherein any layer above the second metal pattern is transparent or the second metal pattern is the outermost layer, such that the second metal pattern is

However, Andry et al. discloses Cathode as a second metal pattern is disposed in the display region, wherein any layer above the second metal pattern is transparent or the second metal pattern is the outermost layer, such that the second metal pattern is capable of reflecting light (page 2, paragraph 17, paragraph 18, Lines 1-3, paragraph 21, Lines 12-15, page 3, paragraph 22 Lines 1-13 teaches cathode also can reflect light).

The reason to combine Andry et al. teaches (AMOLED) dispalyswhich are enhanced by passivating the entire active array surface with an insulating layer, thereby substantially reducing

or eliminating electrical shorts across the organic light emitting diode (OLED) layer from the top electrode to the bottom electrode.

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Andry et al. in the teaching of Gleason Robert E. to be able to have OLED display reducing or eliminating electrical shorts across the organic light emitting diode (OLED) layer from the top electrode to the bottom electrode (page 1, paragraph 2).

Regarding Claim 20, Gleason Robert E. teaches the recognition equipment includes a light source (Col. 7, Lines 53-64), a receiver (Col. 7, Lines 53-55 the photodiodes are receiver), and a signal feedback device (, wherein when light from the light source irradiates the flat panel display (Col. 7, Lines 53-57, photodiode receives lights from OLED, corresponding pixel), the light is reflected by the first and/or second metal pattern (Col. 7, Lines 63-67), the receiver receives a signal of the reflected light (photodiode receives the light Col. 7, Lines 53-58,63-67) and transmits the signal (Col. 8, Lines 25-35) to the signal feedback device (Col. 7, Lines 56-59, Col. 8, Lines 24-56), and the signal feedback device transmits the signal back to the flat panel display (Col. 7, Lines 53-67, Col. 8, Lines 24-56).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kondo, Kenichi (US 20030025659 A1) Light valve device.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

9. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

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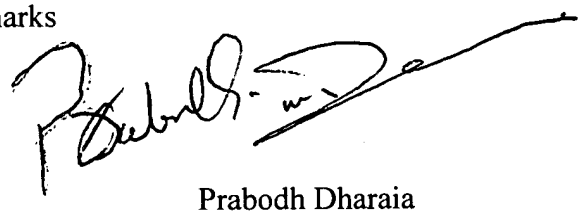
Washington, D.C. 20231



Prabodh Dharaia

Partial Signatory Authority Program

AU 2629

December 22, 2006